|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | ALU Operations |  | LHI |  | LOAD |
| |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  I9 – 11  A2RF  D1 ALU  D2 ALU  ALU T1 | |  | | I3 – 5 A3RF  T1 D3RF | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF | |  | | I0 – 8  SE9 – 16  LS7  LS7  D3RF  I9 – 11  A3RF | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  D1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1 | |  | | T1 MEMDAT (A)  MEMDAT (DO) T2 | |  | | T2 ALU  0 ALU  I9 – 11  A3RF  T2 D3RF | | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | STORE |  | LOAD MULTIPLE |  | STORE MULTIPLE |
| |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  I9 – 11  A2RF  D1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1 | |  | | T1 MEMDAT (A)  D2 MEMDAT(DI) | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF  I9-11  A1RF  D1 MEMDAT(A)  MEMDAT (DO) T2 | |  | | WHILE (PEINPUT IS VALID) {  T2 D3RF  PEOUTPUT A3RF  T2 ALU  +1 ALU  ALU T1 | |  | | T1 T2} | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF  I9-11  A1RF  D1 MEMDAT(A), T2  PEOUTPUT  A2RF | |  | | WHILE (PEINPUT IS VALID) {  T2 MEMDAT(A)  D2MEMDAT(DI)  T2 ALU  +1 ALU  ALU T1 | |  | | PEOUTPUT  A2RF  T1 T2} | | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | BEQ |  | JAL |  | JLR |
| |  |  | | --- | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | | |  | | | I6 – 8  A1RF  I9 – 11  A2RF  D1 EQU  D2 EQU | | |  | | | T1 D3RF  “111” A3RF | “111” A1RF  D1RF ALU  I0 – 5  SE6 – 16  ALU  ALU PC | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3RF  I9-11 A3RF  “111” A1RF  D1RF ALU  I0 – 8  SE9 – 16  ALU  ALU T1 | |  | | T1 D3RF  “111” A3RF | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | I9 – 11  A3RF  T1 D3RF | |  | | I6 – 8  A1RF  D1RF D3RF  “111” A3RF | | |

So our FSM does a lot of work here, the data path only controls a small section of all the happenings. E.g.: the set C and Z flag in AL instructions would also be done by the FSM itself. For the branching R type instructions, such as ADC, ADZ, etc. we have assumed that the addition will be done, only the transfer will be controlled by the FSM, which has access to the flags as well.